di·men·sion (dĭ-mĕn′shən, dī-) *noun*

Abbr. **dim.**

1. A measure of spatial extent, especially width, height, or length.
2. Often **dimensions** . Extent or magnitude; scope: *a problem of alarming dimensions.*
3. Aspect; element: *"He's a good newsman, and he has that extra dimension"* (William S. Paley).
4. *Mathematics.* **a.** One of the least number of independent coordinates required to specify uniquely a point in space or in space and time. **b.** The range of such a coordinate.
5. *Physics.* A physical property, such as mass, length, time, or a combination thereof, regarded as a fundamental measure or as one of a set of fundamental measures of a physical quantity: *Velocity has the dimensions of length divided by time.*

verb, transitive

di·men·sioned, di·men·sion·ing, di·men·sions

1. To cut or shape to specified dimensions.
2. To mark with specified dimensions.

prox·i·mate (pr□k□s□-m□) *adjective*

1. Closely related in space, time, or order; [redacted] See synonyms at close.
2. [redacted]

[

US006251704B1

(12) United States Patent
Ohuchi et al.

(10) Patent No.: US 6,251,704 B1
(45) Date of Patent: Jun. 26, 2001

(54) METHOD OF MANUFACTURING SEMICONDUCTOR DEVICES HAVING SOLDER BUMPS WITH REDUCED CRACKS

(75) Inventors: Shinji Ohuchi; Yoshimi Egawa; Noritaka Anzai, all of Tokyo (JP)

(73) Assignee: Oki Electric Industry Co., Ltd., Tokyo (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 09/285,656

(22) Filed: Apr. 5, 1999

Related U.S. Application Data

(62) Division of application No. 09/167,525, filed on Oct. 7, 1998

(30) Foreign Application Priority Data

Dec. 25, 1997 (JP) 9-357155

(51) Int. Cl.[7] H01L 21/44; H01L 21/45; H01L 21/50; H01L 21/302; H01L 21/461; H01L 23/48; H01L 23/52; H01L 29/40

(52) U.S. Cl. 438/108; 438/613; 438/614; 438/615; 438/713; 257/778

(58) Field of Search 438/108, 613, 438/614, 713, 615; 257/778; 228/179.1

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Primary Examiner—Charles Bowers
Assistant Examiner—Nema Berezny
(74) Attorney, Agent, or Firm—Jones Volentine, L.L.C.

(57) ABSTRACT

A metal is formed at a rear surface of a substrate, the substrate also having a front surface at which a molded semiconductor chip is mounted. The metal pattern is covered with an insulating film, except for at a connecting area. A solder ball is bonded to the connecting area. The area of the metal pattern other than the connecting area inclines toward the substrate and gradually becomes thinner toward the outside thereof. Stress, which is applied to the solder ball, is imparted in a diagonal direction and is dispersed. As a result, the number of occurrences of cracks is reduced, and the solder ball which is used to achieve connection with an external substrate, is effectively prevented from becoming electrically disconnected.

20 Claims, 13 Drawing Sheets

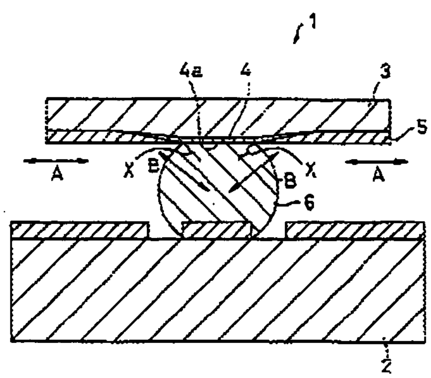


FIG. 7

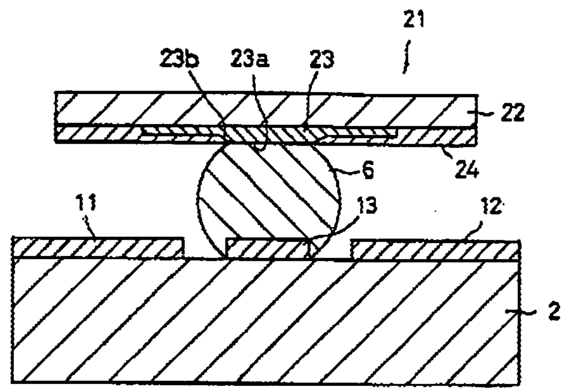
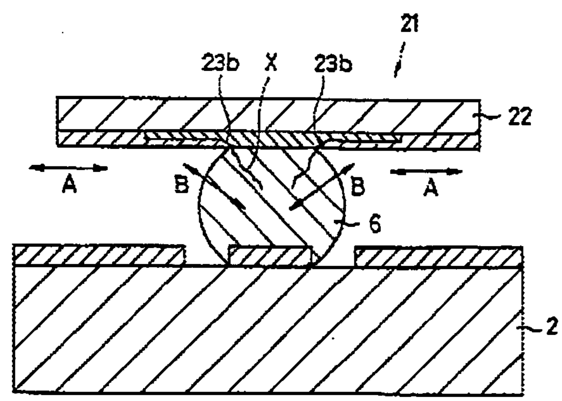


FIG. 8



Ohuchi

METHOD OF MANUFACTURING SEMICONDUCTOR DEVICES HAVING SOLDER BUMPS WITH REDUCED CRACKS

CROSS REFERENCE TO RELATED APPLICATIONS

This is a divisional application of application Ser. No. 09/167,529, filed Oct. 7, 1998, which is hereby incorporated by reference in its entirety for all purposes.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a semiconductor device and a manufacturing method thereof.

2. Description of Related Art

With the rapid advent of portable devices such as mobile phones and IC cards in recent years, and the resulting need for thinner, lighter, more compact resin-sealed semiconductor devices to be mounted in those devices, a great number of means to fulfill such need have been proposed in the prior art. In one such instance, a method for mounting a resin-sealed semiconductor device **101** at an external substrate **102** such as a printed circuit board, as illustrated in FIG. **31**, is proposed.

In the resin-sealed semiconductor device **101** that achieves this mounting state, a mold portion **104** constituted by sealing a semiconductor chip is provided at a front surface of a substrate **103** constituted of an epoxy resin, ceramic or the like and solder balls **105** to function as solder bumps are bonded in advance at specific connecting areas at a rear surface of the substrate **103**. Then, the semiconductor device **101** in this state is placed on the external substrate **102** and the entire assembly is placed in an atmosphere at a temperature ranging approximately from 220 centigrade to 240 centigrade. Thus, the solder balls **105** are at least partially melted so that the semiconductor device **101** can be mounted at the external substrate **102**. Through this mounting method, electrical characteristics with a low capacity and low inductance are achieved.

To describe the structure of the resin-sealed semiconductor device **101** that achieves this mounting state in more detail, in reference to FIG. **32**, a metal pattern **106** formed at a rear surface of the substrate **103** is covered with an insulating film **107** constituted of, for instance, asolder resist, except at a specific connecting area **106***a*, the connecting area **106***a* is set so that it lies flush with a front surface of the insulating film **107** and a surface of the connecting area **106***a* is flat. A solder ball **105** is bonded to the connecting area **106***a*.

When mounting the semiconductor device **101** at the external substrate **102**, the solder ball **105** is aligned at a specific electrode portion **109** formed between insulating layers **108** and **108** and then the entire assembly is placed in a specific heated atmosphere in this state.

However, the following problem manifests with the semiconductor device **101** in the prior art structured as described above in a reliability test which is performed after it is mounted at the external substrate **102**. Namely, during the reliability test in which the semiconductor device is exposed to an atmosphere at room temperature or within the range of −65 centigrade to 150 centigrade, an electrical disconnection sometimes occurs at the solder balls **105**. This is considered to be caused by the difference between the coefficients of thermal expansion of the semiconductor device **101** constituted of the substrate **103** and the mold portion **104** and of the external substrate **102** at which the semiconductor device **101** is mounted, which causes the semiconductor device **101** to be stretched and to contract, as illustrated in FIG. **33**, causing cracks **110** and **111** to be formed at a solder ball **105**, which, in turn, leads to degradation of the electrical characteristics and eventually to disconnection as these cracks **110** and **111** grow to link with each other.

In an examination of the positions at which the cracks **110** and **111** are formed, their patterns and their directions, conducted by the inventors of the present invention, cracks were found to form near the metal pattern **106** to extend in parallel to the metal pattern **106** in most instances. The inventors of the present invention conducted a similar experiment after essentially modifying the shape of the metal pattern connecting area which is bonded with the solder ball, and a great improvement was observed.

SUMMARY OF THE INVENTION

A first object of the present invention, which has been completed by addressing the problem of the semiconductor devices and the manufacturing method thereof in the prior art, is to provide a new and improved semiconductor device with which it is possible to reduce the number of cracks that are formed compared to the prior art and even when they are formed, they are formed and extend in a direction in which disconnection does not readily occur.

A second object of the present invention is to provide a method for manufacturing such a semiconductor device.

In order to achieve the first object of the present invention, in a first aspect of the present invention, a semiconductor device is provided with a substrate having a semiconductor chip at a front surface thereof and a conductor pattern formed at a rear surface of the substrate, i.e., at the mounting surface, with the conductor pattern covered with an insulating film except at specific connecting areas and solder bumps bonded to the connecting areas, which is characterized in that the area of the conductor pattern outside the connecting areas covered by the insulating film inclines toward the substrate, is provided.

An examination conducted by the inventors of the present invention verified that with the area of the conductor pattern such as a metal pattern covered with the insulating film outside the connecting areas made to incline toward the substrate, the rate of cracking is reduced and that even when a crack is formed, it extends almost along the inclination, i.e., in a diagonal direction. These results are assumed to be attributable to the stress at the solder bumps such as solder balls occurring in a diagonal direction and being dispersed, caused by the difference between the coefficients of thermal expansion described earlier. Thus, with the rate of cracking reduced, degradation in the electrical characteristics can be prevented, and furthermore, even when a crack occurs, it extends in a diagonal direction and, consequently, disconnections are greatly reduced too.

In the semiconductor device achieving the advantages described above, the area of the conductor pattern covered by the insulating film outside the connecting areas can be formed so that it becomes gradually thinner, as well as inclining toward the substrate. Furthermore, the portions of the rear surface of the substrate that correspond to the connecting areas may be distended toward the solder bumps, with the insulating film that conforms to the distended shape.

In addition, in order to achieve the object described above, in a second aspect of the present invention, a semiconductor device is provided with a substrate having a semiconductor chip at a front surface thereof and a conduc-

is reduced, and the solder ball which is used to achieve connection with an external substrate, is effectively prevented form becoming electrically disconnected.

20 Claims, 33 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 13

Ohchi

BRIEF SUMMARY:

(1) BACKGROUND OF THE INVENTION

(2) 1. Field of the Invention

(3) The present invention relates to a semiconductor device and a manufacturing method thereof.

(4) 2. Description of Related Art

(5) With the rapid advent of portable devices such as mobile phones and IC cards in recent years, and the resulting need for thinner, lighter, more compact resin-sealed semiconductor devices to be mounted in those devices, a great number of means to fulfill such need have been proposed in the prior art. In one such instance, a method for mounting a resin-sealed semiconductor device 101 at an external substrate 102 such as a printed circuit board, as illustrated in FIG. 31, is proposed.

(6) In the resin-sealed semiconductor device 101 that achieves this mounting state, a mold portion 104 constituted by sealing a semiconductor chip is provided at a front surface of a substrate 103 constituted of an epoxy resin, ceramic or the like and solder balls 105 to function as solder bumps are bonded in advance at specific connecting areas at a rear surface of the substrate 103. Then, the semiconductor device 101 in this state is placed on the external substrate 102 and the entire assembly is placed in an atmosphere at a temperature ranging approximately from 220 centigrade to 240 centigrade. Thus, the solder balls 105 are at least partially melted so that the semiconductor device 101 can be mounted at the external substrate 102. Through this mounting method, electrical characteristics with a low capacity and low inductance are achieved.

→ Col 1, L 36-38

(7) To describe the structure of the resin-sealed semiconductor device 101 that achieves this mounting state in more detail, in reference to FIG. 32, a metal pattern 106 formed at a rear surface of the substrate 103 is covered with an insulating film 107 constituted of, for instance, asolder resist, except at a specific connecting area 106a, the

omitted in the figures showing subsequent embodiments, too.

(4) The semiconductor device 1 has a basic structure in which a metal pattern 4 constituting a conductor pattern is formed at a rear surface of the substrate 3 and a front surface of the metal pattern 4 is covered with an insulating film 5 except for the connecting area 4a. The solder ball 6, which constitutes a solder bump, is bonded at the connecting area 4a. It is to be noted that the planar shape of the connecting area 4a is circular.

(5) The area other than the connecting area 4a in the metal pattern 4 of the semiconductor device 1, i.e., the area covered with the insulating film 5, inclines toward the substrate 3, and furthermore, the thickness of the metal pattern 4 is gradually reduced toward the outside. In addition, the rear surface of the substrate 3 is formed to lie along the shape of the metal pattern 4. In other words, the portion that corresponds to the connecting area 4a is formed in a shape constituting a three-dimensional convex curve toward the solder ball 6.

(6) The semiconductor device 1 in the first embodiment, which is structured as described above is mounted at the external substrate 2 in a manner identical to that employed in the prior art described earlier, by aligning the solder ball 6 at a specific electrode portion 13 formed between insulating layers 11 and 12 that are formed at a front surface of the external substrate 2 and by placing the whole assembly in a specific heated atmosphere to mount the semiconductor device through connection at the solder ball 6.

(7) Even when the semiconductor device 1 in the first embodiment is placed in an atmosphere in which the temperature changes drastically during a reliability test conducted after it is mounted at the external substrate 2 and the difference between the coefficients of thermal expansion at the semiconductor device 1 and the external substrate 2 causes a force in the horizontal direction due to stretching, contraction and the like to be applied to the semiconductor device 1 as indicated with the reciprocal arrows A in FIG. 2, resulting in stress applied to the solder ball 6 connecting the semiconductor device 1 and the external substrate 2, the stress is applied along the inclined portion of the metal pattern 4 as indicated by the reciprocal arrows B in FIG. 2. Moreover, the stress is applied radially over the entire circumference, and therefore, is dispersed.

embodiment of the present invention when it is mounted at an external substrate 2 such as a wiring board, and in order to facilitate the explanation, the illustration of a molded semiconductor chip mounted on a substrate 3 in the semiconductor device 1 is omitted. It is to be noted that an illustration of a molded semiconductor chip on the substrate is omitted in the figures showing subsequent embodiments, too.

(4) The semiconductor device 1 has a basic structure in which a metal pattern 4 constituting a conductor pattern is formed at a rear surface of the substrate 3 and a front surface of the metal pattern 4 is covered with an insulating film 5 except for the connecting area 4a. The solder ball 6, which constitutes a solder bump, is bonded at the connecting area 4a. It is to be noted that the planar shape of the connecting area 4a is circular.

(5) The area other than the connecting area 4a in the metal pattern 4 of the semiconductor device 1, i.e., the area covered with the insulating film 5, inclines toward the substrate 3, and furthermore, the thickness of the metal pattern 4 is gradually reduced toward the outside. In addition, the rear surface of the substrate 3 is formed to lie along the shape of the metal pattern 4. In other words, the portion that corresponds to the connecting area 4a is formed in a shape constituting a three-dimensional convex curve toward the solder ball 6.

(6) The semiconductor device 1 in the first embodiment, which is structured as described above is mounted at the external substrate 2 in a manner identical to that employed in the prior art described earlier, by aligning the solder ball 6 at a specific electrode portion 13 formed between insulating layers 11 and 12 that are formed at a front surface of the external substrate 2 and by placing the whole assembly in a specific heated atmosphere to mount the semiconductor device through connection at the solder ball 6.

(7) Even when the semiconductor device 1 in the first embodiment is placed in an atmosphere in which the temperature changes drastically during a reliability test conducted after it is mounted at the external substrate 2 and the difference between the coefficients of thermal expansion at the semiconductor device 1 and the external substrate 2 causes a force in the horizontal direction due to stretching, contraction and the like to be applied to the semiconductor device 1 as indicated with the reciprocal arrows A in FIG. 2,

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Ohuchi
Col 10, L 19-27

U.S. Patent Jun. 26, 2001 Sheet 1 of 13 US 6,251

FIG. 1

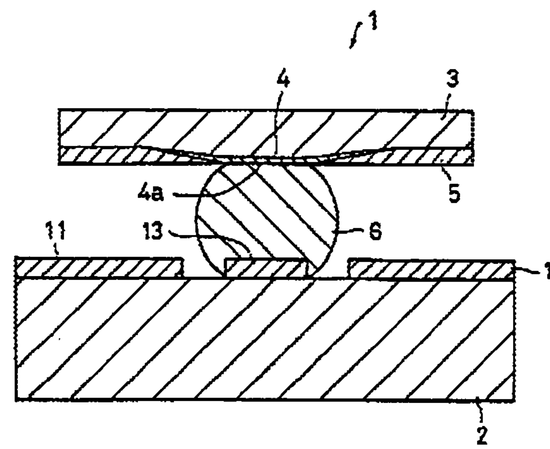
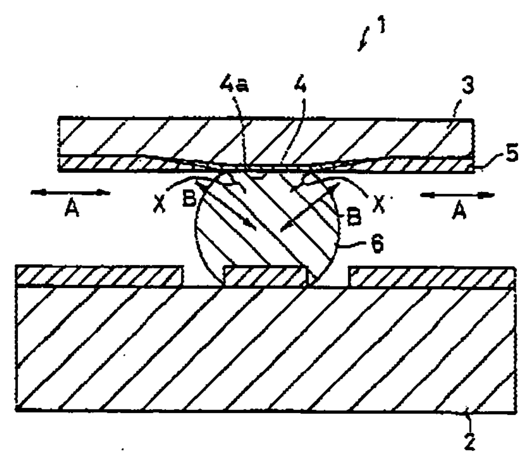


FIG. 2



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(10) Next, as illustrated in FIG. 5, a ceramic plate 15 having an empty portion 15a over the area corresponding to the connecting area 4a is placed at a specific position. Then, pressure is applied to the entire rear surface of the substrate 3 in the direction indicated by the arrows in the figure. This causes the crushed metal pattern 4 to enter a gap "d" formed by the thickness of the metal pattern 4 between the substrate 3 and the ceramic plate 15. In addition, since no force is applied to the empty portion 15a formed at the ceramic plate 15 in correspondence to the connecting area 4a, only the area other than the area at the substrate 3 corresponding to the empty portion 15a is compressed.

(11) Consequently, a structure in which the area other than the connecting area 4a in the metal pattern 4, i.e., the area covered with the insulating film 5 constituted of the ceramic 15 is made to incline toward the substrate 3 and the thickness of the metal pattern 4 is gradually reduced toward the outside, as illustrated in FIG. 6, is achieved. In addition, the rear surface of the substrate 3 achieves a shape that conforms to the shape of the metal pattern 4. After this, a semiconductor chip is mounted at a front surface of the substrate 3 and then is molded with resin or the like. The semiconductor device 1 illustrated in FIG. 1 is then completed by bonding a solder ball 6 to the connecting area 4a through a method in the known art. Thus, the semiconductor device 1 in the first embodiment can be manufactured with a high degree of efficiency.

→ C/1, L 37-43

(12) Next, the semiconductor device in a second embodiment is explained. As the state achieved by mounting the semiconductor device at the external substrate 2 in FIG. 7 clearly illustrates, the members constituting the basic structure at a rear surface of a substrate 22 of the semiconductor device 21 in the second embodiment are identical to those in the semiconductor device 1 in the first embodiment, with a metal pattern 23 constituting a conductor pattern formed at a rear surface of the substrate 22 and an insulating film 24 covering a front surface of the metal pattern 23 except for a connecting area 23a. The planar shape of the connecting area 23a is circular.

(13) A staged portion 23b is formed in the area between the connecting area 23a and the area covered with the insulating film 24 in the metal pattern 23 at the semiconductor device 21, and the staged portion 23b is formed in a tapered shape. In other words, the staged portion

omitted in the figures showing subsequent embodiments, too.

(4) The semiconductor device 1 has a basic structure in which a metal pattern 4 constituting a conductor pattern is formed at a rear surface of the substrate 3 and a front surface of the metal pattern 4 is covered with an insulating film 5 except for the connecting area 4a. The solder ball 6, which constitutes a solder bump, is bonded at the connecting area 4a. It is to be noted that the planar shape of the connecting area 4a is circular.

→ C/10, L 19-27

(5) The area other than the connecting area 4a in the metal pattern 4 of the semiconductor device 1, i.e., the area covered with the insulating film 5, inclines toward the substrate 3, and furthermore, the thickness of the metal pattern 4 is gradually reduced toward the outside. In addition, the rear surface of the substrate 3 is formed to lie along the shape of the metal pattern 4. In other words, the portion that corresponds to the connecting area 4a is formed in a shape constituting a three-dimensional convex curve toward the solder ball 6.

(6) The semiconductor device 1 in the first embodiment, which is structured as described above is mounted at the external substrate 2 in a manner identical to that employed in the prior art described earlier, by aligning the solder ball 6 at a specific electrode portion 13 formed between insulating layers 11 and 12 that are formed at a front surface of the external substrate 2 and by placing the whole assembly in a specific heated atmosphere to mount the semiconductor device through connection at the solder ball 6.

(7) Even when the semiconductor device 1 in the first embodiment is placed in an atmosphere in which the temperature changes drastically during a reliability test conducted after it is mounted at the external substrate 2 and the difference between the coefficients of thermal expansion at the semiconductor device 1 and the external substrate 2 causes a force in the horizontal direction due to stretching, contraction and the like to be applied to the semiconductor device 1 as indicated with the reciprocal arrows A in FIG. 2, resulting in stress applied to the solder ball 6 connecting the semiconductor device 1 and the external substrate 2, the stress is applied along the inclined portion of the metal pattern 4 as indicated by the reciprocal arrows B in FIG. 2. Moreover, the stress is applied radially over the entire circumference, and therefore, is dispersed.

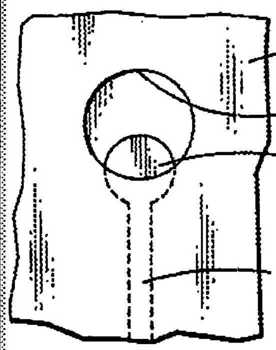

FIG.10

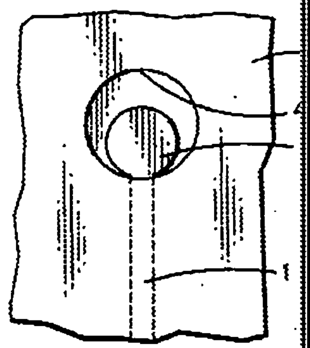

FIG.11

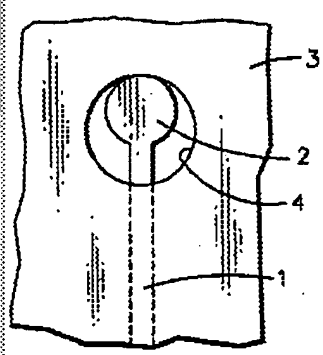

FIG.12

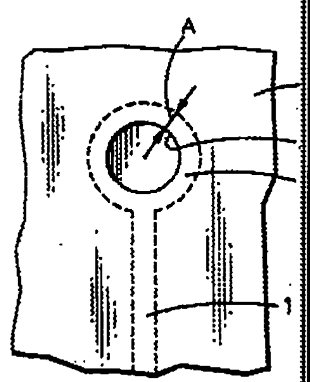

FIG.13

US005517756A

United States Patent [19]

Shirai et al.

[11] Patent Number: 5,517,756
[45] Date of Patent: May 21, 1996

[54] METHOD OF MAKING SUBSTRATE MEMBER HAVING ELECTRICAL LINES AND APERTURED INSULATING FILM

[75] Inventors: Masaharu Shirai, Otsu; Kinshiro Futaoka, Shiga, both of Japan

[73] Assignee: International Business Machines Corporation, Armonk, N.Y.

[21] Appl. No.: 247,530
[22] Filed: May 23, 1994

Related U.S. Application Data

[62] Continuation of Ser. No. 72,561, Jun. 10, 1993, abandoned, which is a division of Ser. No. 859,752, Mar. 30, 1992, Pat. No. 5,252,781.

[30] Foreign Application Priority Data

May 31, 1991 [JP] Japan 3-156222

[51] Int. Cl.⁶ H05K 3/02
[52] U.S. Cl. 29/847; 29/846; 174/255; 174/254
[58] Field of Search .... 29/847, 846; 200/5 A; 174/255, 254

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"Printed Wiring Board", EPO Publication No. JP1094696, Abstract vol. 013332, Apr. 13, 1989, Nakai toru et al.

Primary Examiner—Carl J. Arbes
Attorney, Agent, or Firm—Lawrence R. Fraley

[57] ABSTRACT

In a substrate member (e.g., circuit board), a plurality of openings (15) are formed in an insulating film (14) which covers electric lines (12) formed on a substrate 11, with pad constructing (contacting) portions (13) of selected ones of the electric lines being exposed. In one example, the pad constructing portion (that portion of the pad to which final connection is to occur, e.g., by solder to a semiconductor device), is set to a first dimension (e.g., length) having a dimension less than a corresponding dimension of the original length. The film openings are then set to another dimension having an allowance size larger than a corresponding dimension of the pad constructing portion. The opening is thus of sufficiently large size in comparison to the respective pad being exposed so as to assure effective tolerance compensation for film positioning deviations in at least two (e.g., X and Y) directions as might occur during production of the substrate member.

5 Claims, 4 Drawing Sheets

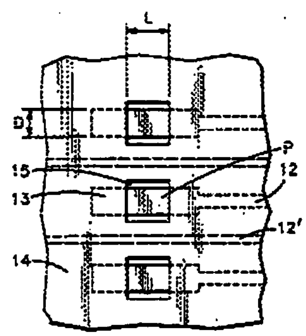

Fig2

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the center of the pad p.sub.1 and the center of the pad p.sub.2 are held (to X, Y). This is because the pad constructing portions 13 are in parallel with each other and the openings 15 are in parallel with each other, the centers of the pads p.sub.1 and p.sub.2 are shifted by only the equal amount in the same direction due to the influence by the positional deviation.

(29) Therefore, all of the pad constructing portions 13 of the electric lines are formed in parallel with each other and all of the openings 15 which are superimposed over the pad constructing portions so as to cross same are also formed in parallel with each other, so that the above operation and effect are obtained.

(30) In the embodiment in FIGS. 8 (and 9), an example in which the pad constructing portions 13 are formed in the front edge portions of the electric lines 12 and thus as extensions thereof to form the pads P has been shown. It is also possible, according to the teachings herein, to enable the films openings to expose, in addition to the front edge portions of the electric lines 12, other portions of the substrate member's electric lines through the insulating film without requiring any additional modifications to the film. That is, the pads can also be formed from the electric lines themselves so long as the area which is required for effective connection can be assured. In this situation, since the electric line itself is extended from the pad portion to a thinner line, allowance is thus provided for the positional deviation of the desired opening. It is, therefore, sufficient to only give the foregoing allowance (2d) to the opening of the insulating film which is superimposed over such electric lines oriented in the pattern of arrays shown therein.

(31) Although the shapes of the pad contacting portions of the electric lines and the openings of the insulating film are not particularly limited, rectangular shapes are desirable.

(32) According to the invention, by making the direction in which there is an allowance of the pad constructing (contacting) portion different from the direction in which there is an allowance for

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US005517756A

United States Patent [19]

Shirai et al.

[11] Patent Number: 5,517,756

[45] Date of Patent: May 21, 1996

[54] METHOD OF MAKING SUBSTRATE MEMBER HAVING ELECTRICAL LINES AND APERTURED INSULATING FILM

[75] Inventors: [illegible]

[73] Assignee: International Business Machines Corporation, Armonk, N.Y.

[21] Appl. No.: [illegible]

[22] Filed: May 23, 1994

Related U.S. Application Data

[62] [illegible]

[30] Foreign Application Priority Data

[51] Int. Cl.[6] [illegible]

[52] U.S. Cl. [illegible]

[58] Field of Search [illegible]

[56] References Cited

U.S. PATENT DOCUMENTS

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"Method of Joining IC Chip Lead", EPO Publication No. [illegible]

"Printed Wiring Board", EPO Publication No. [illegible]

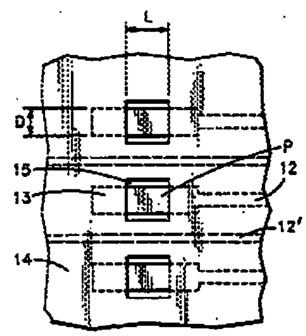
Primary Examiner—Carl J. Arbes

Attorney, Agent, or Firm—Lawrence R. Fraley

[57] ABSTRACT

In a substrate member (e.g., circuit board), a plurality of openings (15) are formed in an insulating film (14) which covers electric lines (12) formed on a substrate 11, with pad constructing (contacting) portions (13) of selected ones of the electric lines being exposed. [illegible]

3 Claims, 4 Drawing Sheets



C6, L 60-63

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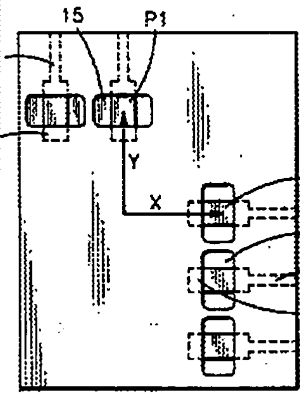

FIG.6

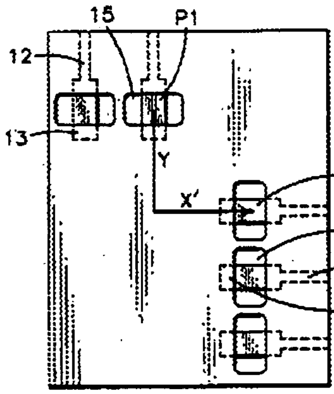

FIG.7

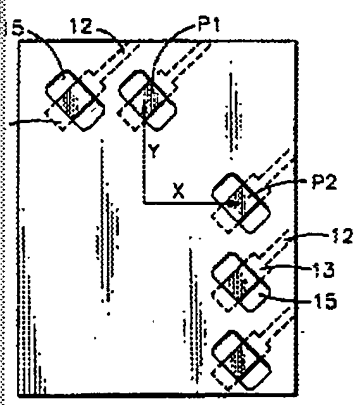

FIG.8

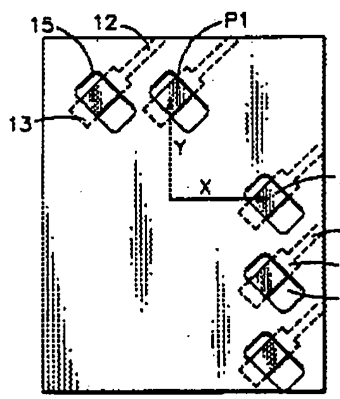

FIG.9

US005517756A

United States Patent [19]

Shirai et al.

[11] Patent Number: 5,517,756
[45] Date of Patent: May 21, 1996

[54] METHOD OF MAKING SUBSTRATE MEMBER HAVING ELECTRICAL LINES AND APERTURED INSULATING FILM

[75] Inventors: Masaharu Shirai, Otsu; Kimihiro Yamanaka, Shiga, both of Japan

[73] Assignee: International Business Machines Corporation, Armonk, N.Y.

[21] Appl. No.: 247,538

[22] Filed: May 23, 1994

Related U.S. Application Data

[63] Continuation of Ser. No. 72,567, Jun. 10, 1993, abandoned, which is a division of Ser. No. 889,752, May 28, 1992, Pat. No. 5,252,781.

[30] Foreign Application Priority Data

May 31, 1991 [JP] Japan 3-129232

[51] Int. Cl.[6] H05K 3/02
[52] U.S. Cl. 29/847; 29/846; 174/255; 174/254
[58] Field of Search .... 29/847, 846; 200/5 A; 174/255, 254

[56] References Cited

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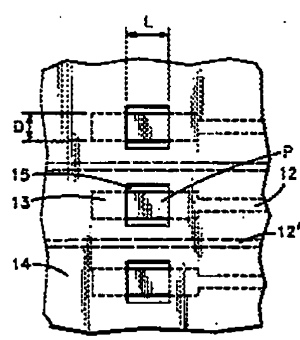
Primary Examiner—Carl J. Arbes
Attorney, Agent, or Firm—Lawrence R. Fraley

[57] ABSTRACT

In a substrate member (e.g., circuit board), a plurality of openings (15) are formed in an insulating film (14) which covers electric lines (12) formed on a substrate 11, with pad constructing (connecting) portions (13) of selected ones of the electric lines being exposed. In one example, the pad constructing portion (that portion of the pad to which final connection is to occur, e.g., by solder to a semiconductor device), is set to a first dimension (e.g., length) having a dimension less than a corresponding dimension of the original length. The film openings are also set to another dimension having an allowance size larger than a corresponding dimension of the pad constructing portion. The opening is thus of sufficiently large size in comparison to the respective pad being exposed so as to assure effective tolerance compensation for film positioning deviations in at least two (e.g., X and Y) directions as might occur during production of the substrate member.

3 Claims, 4 Drawing Sheets



Shirai

METHOD OF MAKING SUBSTRATE MEMBER HAVING ELECTRICAL LINES AND APERTURED INSULATING FILM

The application is a continuation of application Ser. No. 08/075,067, filed Jun. 10, 1993, abandoned, which is a divisional of application Ser. No. 07/859,750 filed on Mar. 30, 1992, now U.S. Pat. 5,252,781.

TECHNICAL FIELD

The invention relates to substrate members (e.g., circuit boards) including electric lines as part thereof and to a method of manufacturing such a substrate member. More particularly, the invention relates to a substrate member and method of making same wherein pads formed in conjunction with said lines and having predetermined areas in a predetermined positional relation are utilized while permitting a relative positional deviation between such pads (also referred to as pad constructing portions) of the electric lines and respective openings within an insulating film also used as part of the substrate member, the film functioning to cover selected portions of the line(s).

DESCRIPTION

In a substrate member (e.g., printed circuit board) including electric lines, such electric (e.g., copper) lines are provided on a dielectric (e.g., fiberglass reinforced epoxy resin) substrate and an electrically insulating film may be provided on the substrate so as to cover the electric lines or portions thereof. To electrically connect the electric lines on the substrate to other circuits or components, openings may be formed in the insulating film in order to expose parts of the electric lines, such exposed line portions also being defined as "pads" (or pad constructing portions).

It is required that such pads be of specified area (large enough) in order to assure the reliability of the electrical connection. Particularly, in a small substrate such as a substrate having electric lines used to support (be coupled to) a semiconductor chip or the like (such exposed areas being extremely small), the exposed areas of the pad must be precisely defined. Moreover, in a flip-chip type of structure (wherein the pads on the substrate and the pads on the semiconductor chip typically used in such members are connected by a metal (e.g., solder) ball, not only are both of the paired pads electrically connected but also the semiconductor chip is physically positioned onto the substrate having such electric pads/lines, such that the area of the pad is also important in terms of providing sufficient strength for the final structure.

In the situation where a position of an opening formed in an insulating film is offset from an electric line pad constructing portion provided, e.g., at a front edge of an electric line, the resulting exposure area of the electric line pad may be too small, such that the reliabilities of any electrical connection and attaching strength may be severely diminished.

Because a process to form an electric line onto the substrate and to precisely orient the insulating film onto the substrate so as to precisely form an opening relative to each line/pad must be sequentially executed (e.g., the lines are formed on the dielectric substrate first, following which the film is positioned thereover), a possibility exists that the positional deviation between the line/pad constructing portion and the respective film opening as mentioned above may be extremely high.

Even if the positional deviation is of a degree such that only a part of the line/pad constructing portion is covered by the insulating film, the problem of the aforementioned poor reliabilities still exists. That is, even in the case where part of the pad constructing portion lies within the film opening, the portion of the insulative film over the electric line may also function as a connecting pad, together with the pad constructing portion. Therefore, the combined pad area fluctuates due to the above positional deviation.

FIGS. 10–13 are provided to better illustrate the above. In FIG. 10, for example, the underlying circuit line 1 terminates in a circular contacting portion (pad) 2 of a predetermined diameter smaller than the respective opening 4 in the dielectric film (3) located thereover. Should the opening be shifted slightly, as in FIG. 11, a relatively large substrate surface area under the opening remains exposed. This is further seen for a positional change as depicted in FIG. 12. To prevent the above, a relatively large, annular pad may be provided (FIG. 13) in combination with a smaller diameter film opening 4. Using such parameters, film positioning deviations (no greater than dimension A) are compensated for to assure that a suitable pad area will always remain exposed. This necessitates, however, the defined provision of large pad sites, further reducing the chance for high density site arrays highly desired in today's information handling systems (computer) environments to which the present invention is particularly suited.

To solve the foregoing and related problems, an improved method of making a substrate member has been developed. It is believed that such a method, and the substrate member resulting therefrom, will constitute a significant advancement in the art.

DISCLOSURE OF THE INVENTION

It is an object of the invention to provide a substrate member having electric lines in which even when a predetermined positional deviation of an opening formed in the member's insulating film relative to a pad constructing portion of the member's electric line(s) occurs, such deviation is acceptable and a pad of a predetermined area can be assured.

It is another object of the invention to provide a method of making a substrate member having electric lines wherein a plurality of pads are formed onto a substrate (e.g., at the end of electric lines), such that even when a positional deviation of the openings in the member's insulation film occurs, as mentioned above, the relative positioning relation between the pads is held relatively constant.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is an exploded perspective view of a substrate member including electric lines according to an embodiment of the invention.

FIG. 2 is a plan view of the substrate member including electric lines according to an embodiment of the invention.

FIG. 3 is a plan view of a substrate including electric lines according to another embodiment of the invention.

FIG. 4 is a representative diagram illustrating a size of an electric line according to the invention.

FIG. 5 is a representative diagram illustrating a size of opening of an insulating film according to the invention.

FIG. 6 is a representative diagram illustrating an arrangement of pads according to one embodiment of the invention.

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US-PAT-NO: 5818697

DOCUMENT-IDENTIFIER: US 5818697 A

TITLE: Flexible thin film ball grid array containing solder mask

---------- KWIC ---------

Application Filing Date - AD (1):
19970321

Detailed Description Text - DETX (12):
The solder mask material should provide for a permanent solder mask and include photosensitive acrylate and methacrylate type solder mask materials, and epoxy based solder masks. The solder mask material can be liquid or a dry film. When liquid, it can be sprayed or screened onto the carrier. An example of a suitable solder mask is Vacrel 8120 available from DuPont. Vacrel 8120 is a photoimageable dry film of about 2 mils thick and is an acrylate based system from polyol acrylate monomers, benzyphenone, ethyl-4-dimethylamino benzoate, N-methyl-2-pyrrolidone and methylene chloride. Other available suitable solder masks are ASM DF, also known as Laminar L-8404; PSR-4000, ASM UV curing epoxy, Grace CM 2001 (version 3302); and Hysol SR8200. ASM DF is a photoimageable, epoxy based dry film of about 2 mils thick. It contains an epoxy resin; propylene glycol methyl ether acetate; filler and an organic antimony salt. PSR-4000 is a liquid photoimageable solder from an epoxy based system containing diethylene glycol monoethyl acetate. Grace CM 2001 (version 3202) is a liquid acrylic ester system which includes an epoxy resin, ethylene glycol monobutyl ether acetate, an acrylated oligomer, a photoinitiater and curing agent. Hysol SR8200 is a flat matte photoimageable solder mask from an epoxy resin and ethylene glycol monobutyl ether acetate. ASM UV curing epoxy is similar to ASM DF except that it is in liquid form containing more diluent.

Current US Cross Reference Classification - CCXR (7):
257/778

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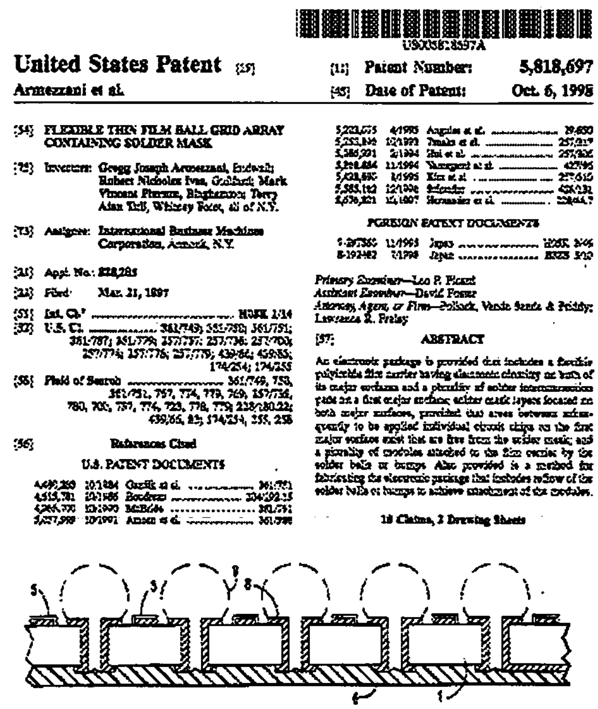
United States Patent [19]
Armezzani et al.
[11] Patent Number: 5,818,697
[45] Date of Patent: Oct. 6, 1998
[54] FLEXIBLE THIN FILM BALL GRID ARRAY CONTAINING SOLDER MASK
[73] Assignee: International Business Machines Corporation, Armonk, N.Y.
[22] Filed: Mar. 21, 1997
[56] References Cited
U.S. PATENT DOCUMENTS
FOREIGN PATENT DOCUMENTS
[57] ABSTRACT
18 Claims, 2 Drawing Sheets

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